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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,350	03/07/2001	Chun Hsiang Lai	JCLA6643	4896

7590
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02/26/2003

EXAMINER

NADAV, ORI

ART UNIT PAPER NUMBER

2811

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/801,350

Applicant(s)

LAI ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 5-12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu (5,869,873)..

Yu teaches in figure 6 an electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit 3, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad 1 and a ground voltage V_{ss} , so as to discharge the electrostatic charges; and an anti-latch-up circuit RC, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source (the line connecting the pad and the internal circuit), the ground voltage V_{ss} , and the third connection terminal of the SCR circuit (the connection between the RC elements and the third

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connection terminal of the SCR circuit is done via transistor 4), whereby an anti-latch-up signal is sent from the sixth connection terminal to the SCR circuit.

Although Yu does not state a voltage source, this feature is inherent in Yu's device as the line connecting the pad and the internal circuit is the voltage source. Furthermore, capacitor C also provides a voltage source to the device (column 5, lines 35-36). Note that the device would not function without a voltage source.

Regarding claim 3, Yu teaches in figure 5 an SCR circuit comprises: a P-type substrate 5; an N well 51, formed in the p-type substrate; a first P+ doped region 56, formed in the P-type substrate and coupled to the ground voltage Vss; a first N+ doped region 54, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage; a second N+ doped region 53, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit; a second P+ doped region 52, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad 1; and a third N+ doped region 57, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source (the line connecting the pad and the internal circuit).

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Regarding claim 4, Yu teaches in figure 6 anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region (via transistor 55) and the ground voltage Vss (via resistor R); and a resistor R, having a first end and a second end, respectively coupled to the voltage source (the line connecting the pad and the internal circuit) via capacitor C and the second N+ doped region (via transistor 55)..

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Ker et al. (5,754,380).

Yu teaches substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

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Ker et al. teach in figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the 1/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the 1/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the 1/O pad; and a second diode, having a first input end and a second input end, respectively connected to the 1/O pad and a voltage source in Yu's device in order to provide better protection for the device against ESD event.

Response to Arguments

5. Applicant argues that EPROM 4 of Yu's device can not provide any voltage to the third terminal of the SCR circuit since it is in a normal off state.

Yu teaches that EPROM 4 triggers the SCR circuit (column 5, line 48).

Triggering is done by applying voltage to the SCR circuit. Therefore, Yu teaches an anti-latch-up circuit providing a voltage to the third terminal of the SCR circuit, as claimed.

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6. Applicant argues that Yu does not teach a voltage source.

Although Yu does not state a voltage source, this feature is inherent in Yu's device, because any voltage applied to the device can be considered as a voltage source. Therefore, the voltage across line connecting the pad and the internal circuit can be considered as a voltage source, and the line connected to capacitor C can be considered as a voltage source (column 5, lines 35-36).

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

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Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read 'Ori Nadav', is positioned above the printed name.

O.N.
February 24, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800